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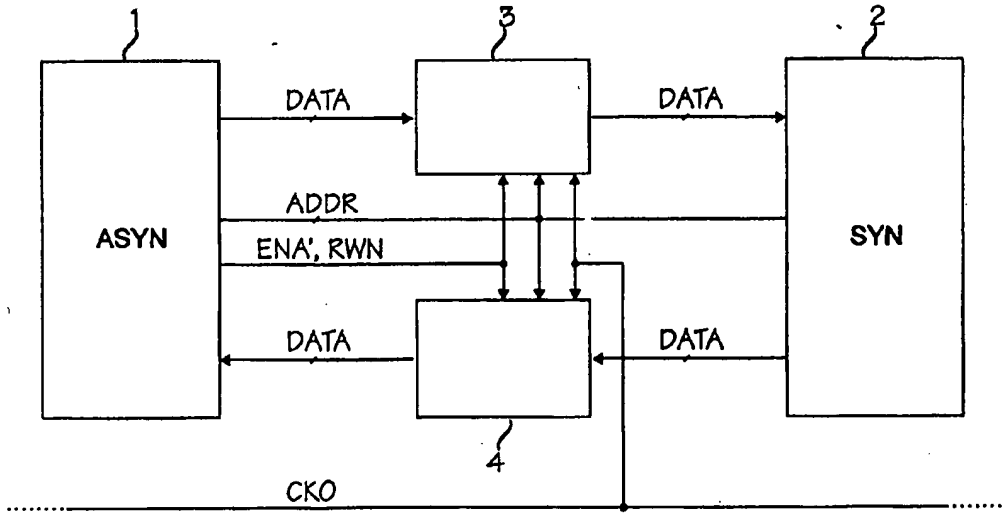

(57) Abstract

Many digital processors have an asynchronous bus controlled by two control signals (ENA', RWN). To interface a synchronous memory to an asynchronous bus, interface logic is required. In the interface (3) for transferring data (DATA) from an asynchronous circuit (1) to a synchronous circuit (2), data to be written are written in an intermediate register (DR) while the timing control signals (ENA', RWN) are being synchronized to the system clock (CKO) by means of flip-flops. Correspondingly, in the interface (4) for transferring data (DATA) from the synchronous circuit (2) to the asynchronous circuit (1), the signal (RWN) indicating a read transaction from the synchronous circuit is synchronized to the system clock by means of a flip-flop circuit.

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Method and apparatus for adapting an asynchronous bus to a synchronous circuit

The present invention relates to an arrangement by which a circuit provided with an asynchronous bus can be adapted to peripheral interface circuits that require a synchronous bus.

Many digital processors have an asynchronous bus which is controlled by two timing control signals. An asynchronous bus may cause difficulties in applications that are strict as far as timing is concerned. The libraries of some producers of Application Specific Integrated Circuits (from hereafter "ASIC circuits") also contain synchronous memories only, or using such a memory instead of an asynchronous memory is otherwise feasible. In order to adapt a synchronous memory to an asynchronous bus, interface logic is required.

In many digital processors, such as the AT&T® signal processor DSP1610, the bus is controlled by two timing control signals. In the figures, they are presented as signals ENA' and RWN. State 0 of the signal ENA' (Enable) indicates that the processor carries out either a read or a write transaction. State 0 of the signal RWN (Read/Write-Not) indicates that the processor is writing to peripheral circuits, and state 1 of the same signal indicates that the processor is reading from the peripheral circuits. If ENA' is "1", the state of the signal RWN' is of no importance.

Formerly, digital processors have been coupled to ASIC circuits by applying both of the control signals ENA' and RWN to peripheral circuits. This results in certain drawbacks. First of all, some circuits only have one line to which a timing control signal can be coupled. In addition, the fact that the transitions of the signals ENA' and RWN have not necessarily been synchronized to the

system clock (CKO) may cause problems in applications that are critical as far as timing is concerned. Furthermore, some ASIC circuit suppliers only have synchronous memories to offer, which means that it is not possible to employ all existing peripheral interface circuits on an asynchronous bus. In addition, an environment requiring two control signals for timing is rather poorly, or not at all, supported by development tools. Test generation is also facilitated if timing takes place with one control signal.

The object of the present invention is to obtain methods and arrangements for eliminating the problems and limitations described above. This object is achieved with the methods according to the characterizing parts of claims 1 and 2, and circuit arrangements according to the characterizing parts of claims 3 and 4.

In the following, the invention will be described in closer detail by means of drawings, in which:

Figure 1 is a block diagram illustration of adapting interfaces according to the invention.

Figure 2 illustrates an adapting interface of the invention for transferring data from an asynchronous circuit to a synchronous circuit.

Figure 3 shows an impulse diagram in a circuit corresponding to Figure 2.

Figure 4 illustrates an adapting interface of the invention for transferring data from a synchronous circuit to an asynchronous circuit.

The positioning of the adapting interfaces of the invention are shown in Figure 1. Between an asynchronous circuit 1 and a synchronous circuit 2 there is arranged an adapting interface 3, which carries out the transfer of data (DATA) from the asynchronous circuit 1 to the synchronous circuit 2, and an adapting interface 4 which carries out the transfer of data in the reverse direction.

According to requirements at any one time, one or both adapting interfaces 3 and 4 of the invention can be used.

In the following, the operation of the adapting interface 3 of the invention is examined on the basis of Figure 2 and the associated pulse diagram 3. The figures present the blocks that are essential to the invention: the asynchronous circuit 1 (e.g. a digital signal processor), the synchronous circuit 2 and the adapting interface 3 in accordance with the invention. In the pulse diagram 3, it is assumed that the write transaction employs a wait state WS and that there is one NOP (No Operation) instruction between two write transactions. In the figures, it is further assumed, without limiting the scope of the invention in any way, that the address bus ADDR of the asynchronous circuit 1 is used to address the whole synchronous memory, which means that at least some bits of the address bus ADDR are used as chip select CS signals for an address comparator EL (Enable Logic). The output of the block EL is "1" in case the most significant bits - equal in number to the width of the address comparator in bits - of the address on the address bus ADDR equal the reference address arranged in the block EL. The figure does not show the design of the address comparator but it is clear that the circuit can be formed of comparator circuits each of which compare one bit on the address bus to a reference value which can be set e.g. by means of adjustable jumper means. The function of the blocks EL and A-DEC is distributed so that the block EL detects that the operation is addressed to the circuit of Figure 2, and the block A-DEC distributes the signal WE' within the circuit of Figure 2. Regarding Figures 2 and 4, it is assumed that the memory address is generated by a peripheral circuit which uses the same clock signal CKO as the other synchronous circuits; therefore, generating the memory address in not disclosed herein. The circuit

generating the memory address may be an autoincrement counter or some other suitable circuit. As far as the present invention is concerned, it is also insignificant where the clock signal CKO is generated.

Referring to Figures 2 and 3, the write cycle of the interface logic according to the invention takes place in the following steps:

1. The switching means 34 detects the moment when at least one of the signals ENA' and RWN (in this example, RWN) changes to "1". If the contents of the address bus simultaneously equal the reference address arranged in the address comparator EL, the data (DATA) are written into an intermediate register DR and the value "1" is written into a flip-flop FF31;

2. On the subsequent rising edge of the clock signal CKO, the value "1" is transferred to the subsequent flip-flop FF32.

3. On the subsequent falling edge of the clock signal CKO, the value "1" is transferred to the subsequent flip-flop FF33. At the same moment, the signal WE' (Write Enable) which is active in state 0 is set to 0. This signal is utilized both for allowing the write transactions to the synchronous memory MEM and functional registers FREG and for resetting the two preceding flip-flops FF31, FF32. The address decoder A-DEC inside the circuit distributes the signal WE' for the circuit section determined by the address bus. In case the write transaction is addressed to the memory, a signal WEB' is produced by the A-DEC to the memory, the WEB' signal being applied to the memory MEM.

4. On the subsequent rising edge of the clock signal CKO, the data on the data bus are written into the memory or the registers.

5. On the subsequent falling edge of the clock signal CKO, the signal WE' is restored to "1", making the

interface ready for the following cycle.

From the pulse diagram 3 illustrating the write transactions to the memory or register, a moment T_x critical to the timing can be seen; if the signal RWN rises to 1 before the signal ENA', as in Figure 3, a transient situation will arise in which the circuit appears to be carrying out a read transaction. What takes place in practise depends on the timing tolerances of the components and on other parameters of the design. As can be seen, such a transient is not present in a signal WE' generated by the circuit according to the invention.

A read transaction can be performed as illustrated in Figure 4. On the basis of the above description on write transactions it can be noted that the synchronization of signals ENA' and RWN to the system clock CKO takes place by means of a flip-flop FF41 and a comparator means 42. If the circuit employs a memory, and a signal OE' (Output Enable) is required for calculating the memory address, the signal can be synchronized to the clock signal CKO. This means that the synchronized signal OE' could be utilized as an ordinary data input for a memory address calculating unit. Other solutions suitable to the application may be employed.

The advantage of the invention described above by means of its preferred embodiment is that only one timing control signal is required for the functional registers. As far as timing is concerned, the circuit arrangement of the invention is less sensitive to delays and other parameters of the design than asynchronous circuits. In addition, even such ASIC circuits that cannot directly be coupled to an asynchronous bus can be coupled to the processor.

Claims

1. Method for transferring data (DATA) from an asynchronous circuit (1) to a synchronous circuit (2) in a system which comprises a system clock (CKO) and in which the asynchronous circuit (1) comprises at least a signal (ENA') indicating data transfer and a signal (RWN) indicating the direction of data transfer, c h a r a c t e r i z e d in that it comprises the following steps:

in response to the signal (ENA') indicating data transfer being active, and to the signal (RWN) indicative of the data transfer direction indicating data transfer from the asynchronous circuit (1) to the synchronous circuit (2), a first switching means (FF31) is set and the data (DATA) are written into an intermediate register (DR);

(i) in response to setting the first switching means (FF31), a second switching means (FF32) is set at the subsequent state transition of the system clock (CKO);

(ii) in response to setting the second switching means (FF32), a third switching means (FF33) is set at the subsequent state transition of the system clock (CKO) ;

(iii) in response to setting the third switching means (FF33), the data (DATA) are written from the intermediate register (DR) to the synchronous circuit (2), and the first and second switching means (FF31; FF32) are reset at the subsequent state transition of the system clock (CKO).

2. A method for transferring data (DATA) from a synchronous circuit (2) to an asynchronous circuit (1) in a system which comprises a system clock (CKO) and in which the asynchronous circuit (1) comprises at least a signal (ENA') indicating data transfer and a signal (RWN) indicating the direction of data transfer,

c h a r a c t e r i z e d by the method comprising the following steps:

(i) in response to the signal (RWN) indicative of the direction indicating data transfer from the synchronous circuit (2) to the asynchronous circuit (1), a switching means (FF41) will be set at the subsequent state transition of the system clock (CKO);

(ii) in response to setting the switching means (FF41) and to the signal (ENA') which indicates data transfer being simultaneously active, as well as the signal (RWN) indicative of the direction indicating data transfer from the synchronous circuit (2) to the asynchronous circuit (1), the data (DATA) are transferred from the synchronous circuit (2) to the asynchronous circuit (1).

3. An apparatus (3) for transferring data (DATA) from an asynchronous circuit (1) to a synchronous circuit (2) in a system which comprises a system clock (CKO) and in which the asynchronous circuit (1) comprises at least a signal (ENA') indicating data transfer and a signal (RWN) indicating the direction of data transfer, c h a r a c t e r i z e d by comprising:

a detector (34), which indicates that the signal (ENA') indicative of data transfer is active, and that the signal (RWN) indicative of the data transfer direction indicates data transfer from the asynchronous circuit (1) to the synchronous circuit (2);

a first switching means (FF31) responsive to the detector (34), the first switching means being set, and an intermediate register (DR) into which the data (DATA) will be written at the next state transition of the system clock (CKO);

a second switching means (FF32) which is set at the next state transition of the system clock (CKO) in response to setting the first switching means (FF31);

a third switching means (FF33) which is set at the next state transition of the system clock (CKO) in response to setting the second switching means (FF32), and

a fourth switching means (A-DEC) which in response to setting the third switching means (FF33) causes the data (DATA) to be written from the intermediate register (DR) to the synchronous circuit (2).

4. An apparatus (4) for transfer of data (DATA) from a synchronous circuit (2) to an asynchronous circuit (1) in a system which comprises a system clock (CKO) and in which the asynchronous circuit (1) comprises at least a signal (ENA') indicative of data transfer and a signal (RWN) indicative of the direction of data transfer, c h a r a c t e r i z e d by comprising:

a first switching means (FF41), which is set at the next state transition of the system clock (CKO) in response to the signal (RWN) indicative of the direction indicating transfer of data from the synchronous circuit (2) to the asynchronous circuit (1);

second switching means (43, 44) which transfer the data from the synchronous circuit (2) to the asynchronous circuit (1) in response to setting the first switching means (FF41) and to the signal (ENA') which indicates data transfer simultaneously being active, as well as the signal (RWN) indicative of the direction indicating data transfer from the synchronous circuit (2) to the asynchronous circuit (1).

5. A method as claimed in claim 1, c h a r a c t e r i z e d by any one of the steps (i)-(iii) in addition comprising the condition:

the contents of the address bus (ADDR) equal the reference address arranged in the address comparator (EL) as far as those bits of the address bus (ADDR) are concerned that have a corresponding bit in the address comparator (EL).

6. An apparatus (3) as claimed in claim 3, c h a r a c t e r i z e d in that it further comprises:

an address comparator (EL) which is coupled to the address bus (ADDR), and to which at least one of the first, second or third switching means (FF31-FF33) or the intermediate register (RD) is in addition responsive to.

FIG. 1

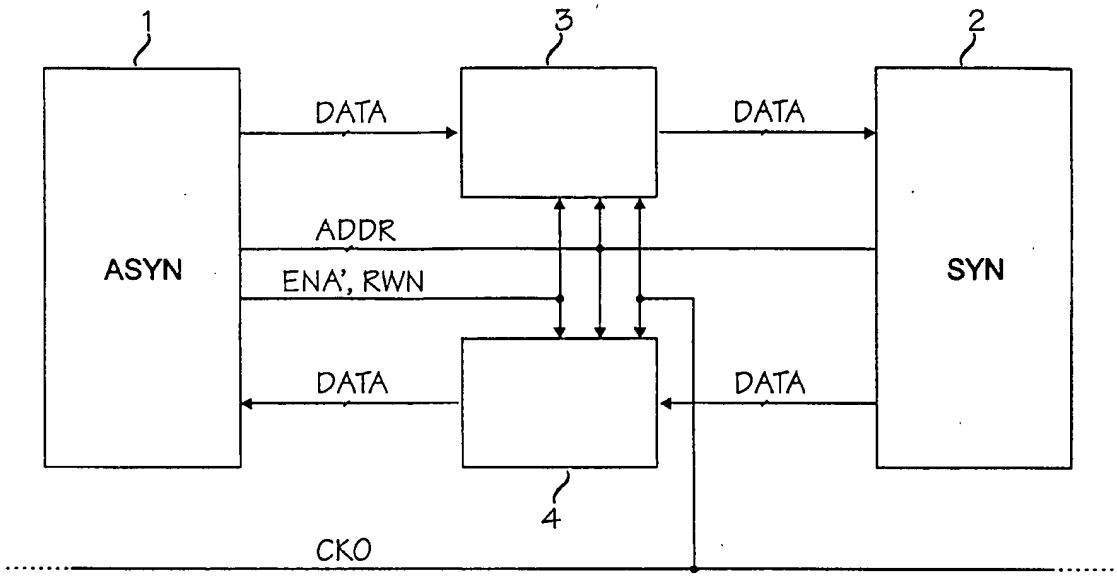
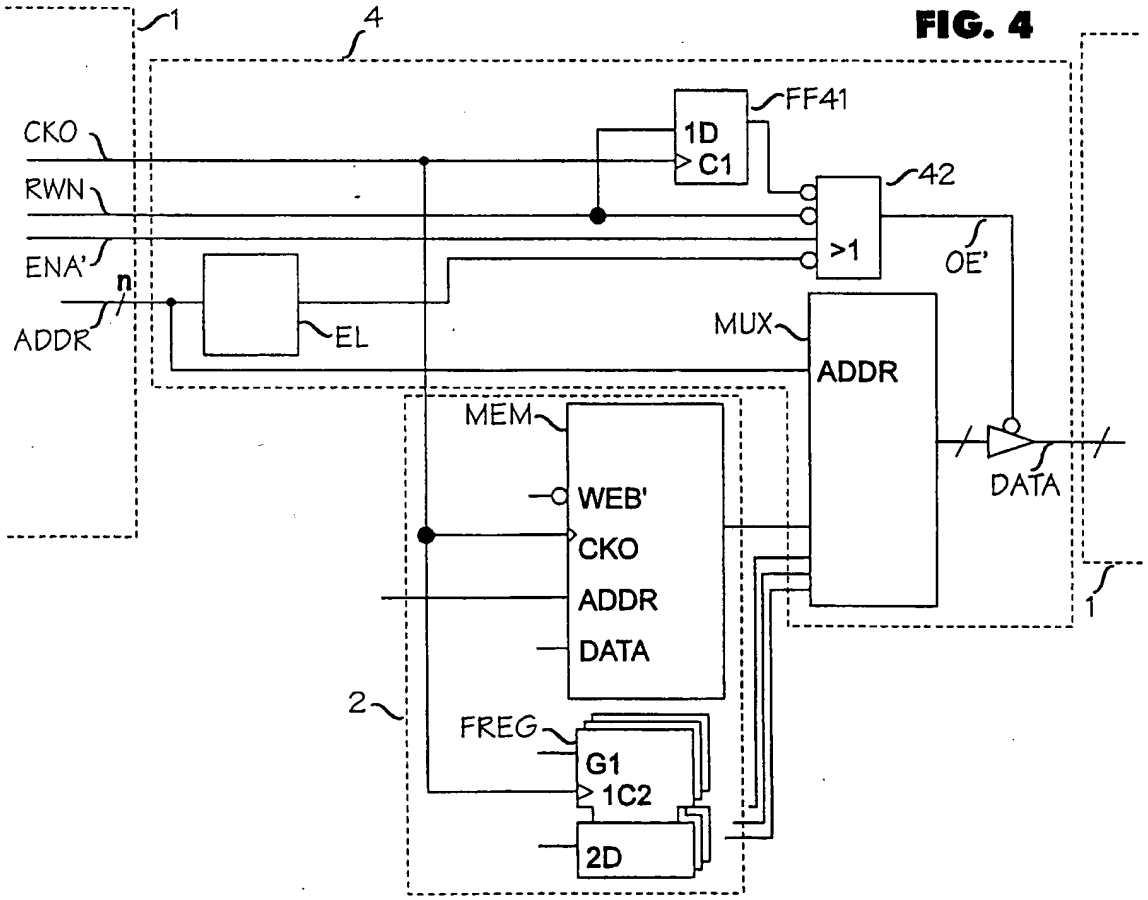
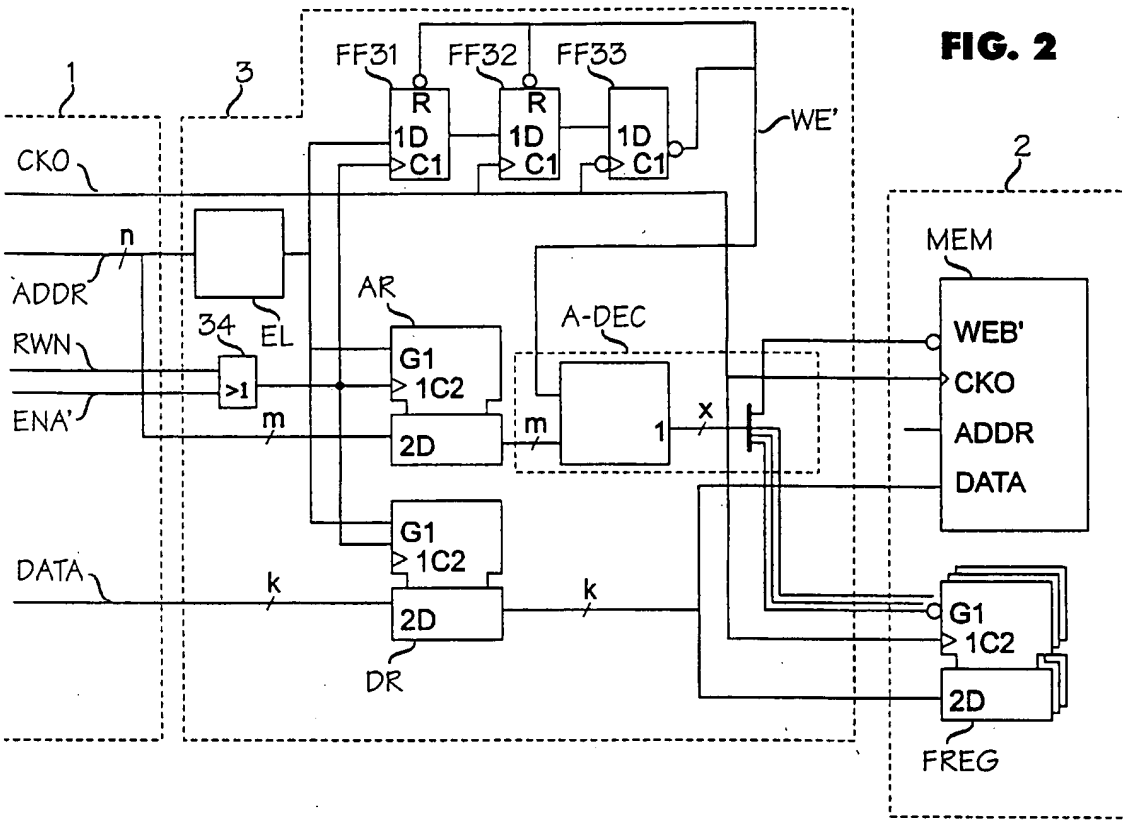

1
3
2
DATA
DATA
ADDR
ASYN
ENA', RWN
SYN
DATA
DATA
4
CKO

FIG. 4


1
4
CKO
RWN
ENA'
n
ADDR
EL
FF41
1D
C1
42
>1
OE'
MUX
ADDR
MEM
WEB'
CKO
ADDR
DATA
DATA
1
2
FREG
G1
1C2
2D


1
3
2
FF31
FF32
FF33
R
1D
C1
WE'
CKO
n
ADDR
RWN
ENA'
34
EL
>1
AR
G1
1C2
2D
m
A-DEC
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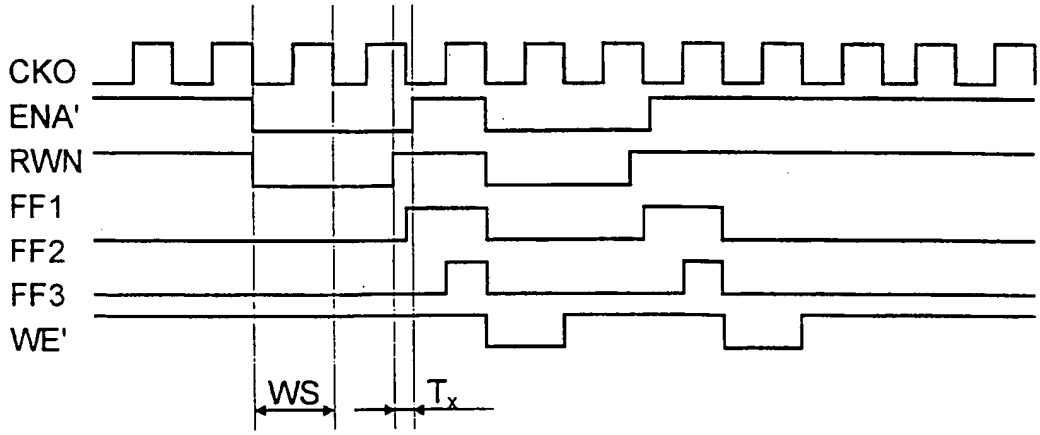
x
MEM
WEB'
CKO
ADDR
DATA
DATA
k
DR
FREG

FIG. 2

FIG. 3


CKO
ENA'
RWN
FF1
FF2
FF3
WE'
WS
T_x